What is claimed is:

1. An integrated circuit, comprising:

one or more memory cells, each memory cell comprising first and second p-channel transistor and first and second n-channel transistors configured as cross-coupled logic inverters between first and second reference voltage levels during a normal mode of operation; and

power control circuitry coupled to a source terminal of the first p-channel transistor of each memory cell, for providing to the first p-channel transistors the first reference voltage level during the normal mode of operation, and causing a first voltage less than the first reference voltage level to appear at the source terminal of the first p-channel transistors during a data corruption mode of operation wherein data stored in the one or more memory cells is corrupted.

2. The integrated circuit of claim 1, wherein the power control circuitry is coupled to a source terminal of the second p-channel transistor of each memory cell, for providing to the first p-channel transistor the first reference voltage level during the normal mode of operation, and the first voltage during the data corruption mode of operation.

3. The integrated circuit of claim 1, wherein the power control circuitry is coupled to a source terminal of at least one of the first and second n-channel transistor, for providing to the at least one of the first and second n-channel transistors the second reference voltage level during the normal mode of operation, and for causing a second voltage greater than the second reference voltage level to appear on the source terminal of at least one of the first and second n-channel transistors during the data corruption mode of operation.

4. The integrated circuit of claim 3, wherein the at least one of the first and second n-channel transistor has a drain terminal coupled to a drain terminal of the second p-channel transistor.

5. The integrated circuit of claim 3, wherein, during the data corruption mode of operation, the power control circuitry pulses the source terminal of the first p-channel transistor of each memory cell to the first voltage, and pulses the source terminal of the at least one of the first and second n-channel transistors to the second voltage, the pulses partially overlapping.

6. The integrated circuit of claim 5, wherein, during the data corruption mode of operation, a leading edge of the pulse corresponding to the first p-channel transistor occurs prior to a leading edge of the pulse corresponding to the at least one of the first and second n-channel transistors.

7. The integrated circuit of claim 6, wherein, during the data corruption mode of operation, a trailing edge of the corresponding to the first p-channel transistor occurs prior to a trailing edge of the pulse corresponding to the at least one of the first and second n-channel transistors.

8. The integrated circuit of claim 5, wherein the power control circuitry temporarily shorts the source terminal of the first p-channel transistor in each memory cell to the source terminal of the at least one of the first and second n-channel transistors in each memory cell.

9. The integrated circuit of claim 8, wherein the power control circuitry comprises at least one first control transistor coupled between the source terminal of the first p-channel transistor of each memory cell to the source terminal of the at least one of the first and second n-channel transistors of each memory cell.

10. The integrated circuit of claim 8, wherein the power control circuitry further comprises at least one second control transistor coupled between the first reference voltage level and the source terminal of the first transistor of each memory cell, and at least one third control transistor coupled between the second reference voltage level and the source terminal of the at least one of the first and second n-channel transistors of each memory cell.

11. The integrated circuit of claim 1, wherein the first voltage is the second reference voltage level.

12. The integrated circuit of claim 1, wherein the first voltage is a voltage resulting from the source terminal of the first p-channel transistor of each memory cell being in an undriven state during the data corruption mode of operation.

13. The integrated circuit of claim 1, wherein each memory cell further comprises at least one pass gate transistor having a conduction terminal coupled to at least one bit line and a control terminal coupled to a word line, and the power control circuitry drives the bit lines to a voltage corresponding to a predetermined logic value and drives each word line to a voltage to activate each pass gate transistor during the data corruption mode of operation when the source terminal of the first p-channel transistor of each memory cell is at the first voltage.

14. A method of corrupting data values stored in a plurality of memory cells coupled between at least one first node and at least one second node, the method comprising:

decoupling the at least one first node from a first reference voltage level and causing a first voltage less than the first reference voltage level to appear on the at least one first node; and

following the step of decoupling, driving the at least one first node towards the first reference voltage level.

15. The method of claim 14, further comprising driving the at least one second node to a second reference voltage level during the step of driving the at least one first node.

16. The method of claim 15, further comprising decoupling, during at least a portion of the time the at least one first node is decoupled from the first reference voltage level and prior to the step of driving the at least one second node, the at least one second node from the second reference voltage level and causing a second voltage greater than the second reference voltage level to appear on the at least one second node.

17. The method of claim 16, wherein the step of causing a second voltage comprises driving the at least one second node to the second voltage.

18. The method of claim 16, wherein the second voltage is the first reference voltage level.

19. The method of claim 16, wherein the step of decoupling the at least one second node occurs after the step of decoupling the at least one first node.

20. The method of claim 16, further comprising shorting the at least one first power supply node to the at least one second power supply node following the steps of decoupling the at least one first power supply node and the at least one second power supply node.

21. The method of claim 15, wherein the first voltage is the second reference voltage level.

22. The method of claim 14, wherein the step of causing a first voltage comprises driving the at least one first power supply node to the first voltage.

23. A system, comprising:

a processing unit; and

one or more memory cells coupled to the processing unit, each memory cell capable of storing one or more data values therein and being coupled to first and second power supply nodes; and

power control circuitry, coupled to the one or more memory cells, for placing a first reference voltage on the first power supply node and a second reference voltage on the second power supply node during a normal mode of operation, and causing a first voltage less than the first reference voltage to appear on the first power supply node during a data corruption mode of operation wherein the one or more data values stored in each of the one or more memory cells are corrupted.

24. The system of claim 23, wherein the first voltage is the second reference voltage.

25. The system of claim 23, wherein each memory cell comprises first and second p-channel transistors and first and second n-channel transistors configured as a logic inverter during the normal mode of operation, the first p-channel transistor having a source terminal coupled to the first power supply node.

26. The system of claim 25, wherein a source terminal of the second p-channel transistor of each memory cell is coupled to a third power supply node, the third power supply node having the first reference voltage during the normal and data corruption modes of operation.

27. The system of claim 26, wherein the power control circuitry comprises a logic inverter having an output coupled to the first power supply node.

28. The system of claim 26, wherein the power control circuitry comprises a transistor coupled between a system power line and the first power supply node.

29. The system of claim 25, wherein a source terminal of the second p-channel transistor of each memory cell is coupled to the first power supply node.

30. The system of claim 25, wherein a source terminal of the second n-channel transistor of each memory cell is coupled to the second power supply node, and a source terminal of the first n-channel transistor of each memory cell is coupled to a fourth power supply node, the fourth power supply node having the second reference voltage during the normal and data corruption modes of operation.

31. The system of claim 23, wherein the power control circuitry places the second reference voltage on the second power supply node during the normal mode of operation and causes a second voltage greater than the second reference voltage to appear on the second power supply node during the data corruption mode of operation.

32. The system of claim 31, wherein the second voltage is the first reference voltage.

33. The system of claim 31, wherein the power control circuitry comprises a first transistor coupled between the first power supply node and the second power supply node, the transistor being activated during a portion of the data corruption mode of operation and deactivated during the normal mode of operation.

34. The system of claim 33, wherein the power control circuitry comprises a second transistor coupled between the first power supply node and the second reference voltage, and a third transistor coupled between the second power supply node and the first reference voltage, the second and third transistors being activated during the data corruption mode of operation and deactivated during the normal mode of operation.

35. The system of claim 34, wherein during the data corruption mode of operation, the first transistor is activated prior to the second and third transistors being activated.

36. The system of claim 31, wherein the power control circuitry comprises a first transistor coupled between a first external voltage supply line and the first power supply node, and a second transistor coupled between a second external voltage supply line and the second power supply node, the first and second transistors being activated during the normal mode of operation and deactivated during at least a portion of the data corruption mode of operation.